

**REMARKS**

Claims 1-24 are all the claims pending in the present application. Applicants thank the Examiner for indicating that claims 5-10, 12-19, and 21-24 contain allowable subject matter and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.<sup>1</sup> In summary, the Examiner withdraws the previous rejections of the claims over previously applied references Sasaki et (US Patent No. 4,942,556) and Cloud et al. (US Patent No. 6,199,251), however the Examiner applies a new reference to support the rejections of the claims. Specifically, claims 1-4, 11, and 20 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Walley et al. (US Patent No. 6,421,283).

A brief description of the new applied reference is as follows.

Walley is directed to a typical integrated circuit device that includes a central processing unit (CPU), trap and patch (T & P) logic circuits and registers. A predetermined number of memory locations in the RAM are allocated for defective memory cell replacement. When power is turned on or the system is reset, the CPU executes a program stored in ROM which identifies defective RAM locations on the fly and loads the trap and path circuits and registers with the defective addresses and the replacement or patch RAM locations (addresses). When the CPU reads or writes to the bad RAM good RAM memory location for the reading and writing operations. In this manner, virtual defective RAM replacement is transparent to the CPU.

With respect to independent claim 1, Applicants submit that Walley does not disclose or suggest at least, "replacing defective cells in the memory with spare memory provided in the

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<sup>1</sup> Claim 18 is an independent claim, therefore Applicants respectfully request that the Examiner indicate that claims 18 and 19 are allowed.

memory controller when there is a request for access to the defective cells of the memory,” as recited in claim 1. The Examiner cites col. 4., lines 20-25 of Walley as allegedly satisfying the above-quoted feature of claim 1. It appears that the Examiner believes that the T&P logic circuit 308 corresponds to the claimed memory controller. Based on this understanding, it is clear that the above-quoted limitation is not satisfied by Walley at least because the T&P logic circuit 308 does not contain therein the spare memory that is to replace the defective cells. At least based on the foregoing, Applicants submit that Walley clearly does not anticipate claim 1.

Applicants submit that independent claim 3 is patentable at least based on reasons similar to those set forth above with respect to claim 1

Applicants submit that dependent claims 2, 4, and 11 are patentable at least by virtue of their respective dependencies. Applicants submit that claim 20 is patentable at least by virtue of its dependency from allowable claim 18.

Further, with respect to independent claim 3, the Examiner cites “fig. 1, 4, 304” as allegedly satisfying the claimed memory scan controller. First, Applicants believe that the Examiner intended to cite Figure 3, as there is no element 304 in Figure 1. Further, the element 304 of Figure 3 is described as read only memory (ROM) 304, and is not described as a memory scan controller. Therefore, at least based on the foregoing, Applicants submit that independent claim 3 is patentable distinguishable over Walley.

With respect to the rejection of dependent claim 11, the Examiner cites col. 4, lines 32-35 as allegedly satisfying the features set forth in this claim. Upon Applicants’ review of Walley, this reference only describes that ROM 304 could cause the CPU to begin its basic operation when the RAM test is routine is finished. There is no specific mention in Walley of how a RAM

test routine is finished. Specifically, there is no disclosure or suggestion in Walley that a checking is determined complete by the scanning for deactivation of a scan signal. The Examiner has obviously utilized impermissible hindsight reasoning in concluding that the features of claim 11 are satisfied by Walley.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

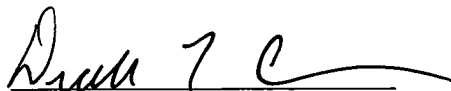
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**23373**

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